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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/689,602

10/22/2003

Yoshiaki Ikematsu

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01/12/2005

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EXAMINER

KENNEDY, JENNIFER M

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/689,602

Applicant(s)

IKEMATSU ET AL.

Examiner

Jennifer M. Kennedy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 October 2003.  
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-6 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/22/2003.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitations "removing the mask film simultaneously with removing the mask film by CMP, using the silicon nitride film as a stopper film". It is unclear what two steps are being done simultaneously. It appears that the claim requires that the mask is removed while the mask is removed with CMP. Claim 3 is rejected for being dependent on claim 2.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Shuichi (JP-2001/237420).

Shuichi discloses the method of manufacturing a semiconductor device having a gate electrode comprising:

forming a gate insulating film (2) on a substrate;  
forming an electrode-constituting film (3) for constituting a gate electrode on the gate insulating film;  
forming a silicon nitride film (4) on the electrode constituting film;  
forming a mask film (6) of the same material as the material of the electrode constituting film, on the silicon nitride film;  
forming a resist pattern (6a) on the mask film;  
patterning the mask film using the resist pattern as a mask to form a patterned mask film (see Figure 2); and  
patterning the silicon nitride film and the electrode-constituting film (see Figures 3 a-c and Figures 6a-c), and,  
simultaneously removing the mask film, by dry etching, using the patterned mask film as a mask (see [0038]).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shuichi (JP-2001/237420) in view of Kim et al. (U.S. Patent No. 6,719,808).

In re claim 1, Shuichi discloses the method of manufacturing a semiconductor device having a gate electrode comprising:

- forming a gate insulating film (2) on a substrate;

- forming an electrode-constituting film (3) for constituting a gate electrode on the gate insulating film;

- forming a silicon nitride film (4) on the electrode constituting film;

- forming a mask film (6) on the silicon nitride film;

- forming a resist pattern (6a) on the mask film;

- patterning the mask film using the resist pattern as a mask to form a patterned mask film (see Figure 2); and

- patterning the silicon nitride film and the electrode-constituting film by dry etching using the patterned mask film as a mask (see Figures 3 a-c and Figures 6a-c and [0038]), and,

- removing the mask film, using the silicon nitride film as a stopper film after patterning the electrode constituting film (see Figures 3 a-c and Figures 6a-c and [0038]).

Shuichi discloses the method as claimed and rejected above, including the method of removing the mask film by a dry etching technique, but does not disclose the

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method wherein removing the mask film is done by CMP. Kim et al. discloses the method of removing polysilicon used as a mask by either a dry etch technique or CMP (see column 1, lines 55-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the polysilicon of Shuichi by the method of Kim et al. because as Kim et al. teaches dry etching and CMP are interchangeable and conventional in the art and CMP allows removal of unwanted masking material with high etch selectivity.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuichi (JP-2001/237420) in view of Kim et al. (U.S. Patent No. 6,719,808) and Park et al. (U.S. Patent No. 6,723,655).

In re claim 2, Shuichi and Kim et al. disclose the method as claimed and rejected above including the method of removing the mask film by CMP, but do not disclose the method forming an interlayer insulating film after patterning the electrode constituting film, forming contact holes in the interlayer insulating film, forming a conductive film over all of the substrate, including in the contact holes, wherein contact plugs are formed in the contact holes in the interlayer insulating film.

Park et al. disclose the method forming an interlayer insulating film (27) after patterning the electrode constituting film, forming contact holes (see Figure 5) in the interlayer insulating film, forming a conductive film (31) over all of the substrate, including in the contact holes, wherein contact plugs are formed in the contact holes in the interlayer insulating film (see Figure 7).

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the an interlayer insulating film after patterning the electrode constituting film, form contact holes in the interlayer insulating film, form a conductive film over all of the substrate, including in the contact holes, wherein contact plugs are formed in the contact holes in the interlayer insulating film to form connections for devices formed above that allow for a highly integrated circuit.

In re claim 3, the combined Shuichi, Kim et al. and Park et al. disclose the method wherein the mask film is the same material as the contact plugs (mask of Shuichi is polysilicon, contact plugs of Park et al. is polysilicon)

In re claim 4, the combined Shuichi, Kim et al. do not disclose the method further comprising forming wirings on the patterned silicon nitride film.

Park et al. discloses the method of forming wirings on the patterned silicon nitride film (33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form wirings on the patterned silicon nitride film to form connections for devices formed above that allow for a highly integrated circuit.

Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shuichi (JP-2001/237420) in view of Park et al. (U.S. Patent No. 6,723,655).

In re claim 6, Shuichi discloses the method as claimed and rejected above, but does not disclose the method further comprising forming wirings on the patterned silicon nitride film.

Park et al. discloses the method of forming wirings on the patterned silicon nitride film (33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form wirings on the patterned silicon nitride film to form connections for devices formed above that allow for a highly integrated circuit.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Jennifer M. Kennedy  
Patent Examiner  
Art Unit 2812

jmk